REMARKS

Claims 1, 2, 4 to 6 were pending when last examined. Applicant has amended claim 1.

§102 Rejections

The Examiner rejected claims 1, 3 to 8, and 12 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,479,641 ("Nadir et al."). Addressing Applicant's argument filed on October 15, 2004, the Examiner stated,

> As admitted by applicant, Nadir teaches invalidating a cache line for tag parity errors. The claim is presented in the alternative. Nadir reads on the situation where a cache line is invalidated for tag parity errors by applicant's own admission and therefore reads on the claim.

November 24, 2004 Final Office Action, p. 5.

Applicant has amended claim 1 to remove the alternative language. Amended claim 1 now recites:

> 1. A method for error protection of a cache memory, wherein each entry in a tag memory and a data store within the cache memory associates with a parity bit, comprising:
>
> (a) providing a read request to a system memory associated with the cache memory, the read request correlating to an entry in the tag memory and the data store;
>
> (b) checking the parity bit associated with the correlated entry in the tag memory and the parity bit associated with the correlated entry in the data store;
>
> (c) if an error is detected in the correlated entry in the data store, declaring a miss and invalidating the correlated entry in the data store.

Amended claim 1 (emphasis added). As described in the response filed on October 15, 2004, Nadir et al. only discloses invalidating a cache line for tag parity errors but not data parity errors. Accordingly, claim 1 is patentable over Nadir et al. for reciting "if an error is detected in the correlated entry in the data store, declaring a miss and invalidating the correlated entry in the data store."

Applicant notes that the Examiner may wish to cite U.S. Patent No. 5,345,582 ("Tsuchiya") against claim 1. Applicant finds that Tsuchiya does not disclose "invalidating the correlated entry in the data store" as recited in claim 1. However, Tsuchiya does states that "[i]f error is a permanent one, the offending portion of the attached memory may be degraded by using techniques known in the art so that it will not be used again." Tsuchiya, col. 5, lines 51 to 54.

Claims 4 to 6 depend from claim 1 and are patentable over Nadir et al. for at least the same reasons as amended claim 1.

§ 103 Rejection

The Examiner rejected claim 2 under § 103(a) as being unpatentable over Nadir et al. in view of U.S. Patent No. 5,832,250 ("Whittaker").

Claim 2 depends from amended claim 1 and is patentable over the combination of the cited references for at least the same reasons as claim 1.

In summary, claims 1, 2, 4 to 6 were pending when last examined. Applicant has amended claim 1. For the above reasons, Applicant respectfully requests allowance of claims 1, 2, 4 to 6. Should the Examiner have any questions, please call the undersigned at (408) 382-0480 x206.

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Respectfully submitted,

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